SSIE Summer School Report: GaN Power Converters

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***Abstract*—This report will provide an overview for designing high efficiency power converters and inverter using novel Wide Bandgap Semiconductors. An overview of the advantages by using those power switches will be provided. The last part of the report is dedicated to a possible application of high frequency converters, namely the class E inverter.**

I. Introduction

THE power electronic market is expected to have a strong growth in the very next years, driven by established applications, as rail traction or motor drives, or by novel applications, as Electric Vehicles or the Wireless Smart Powering of pervasive and IoT systems. The need of high efficiency and of weight, size, and cost reduction is driving the research for novel materials and devices which could sensibly change the electronics of the future.

Wide Band Gap (WBG) Semiconductor Market is currently governed by two materials, the Gallium Nitride (GaN) and the Silicon Carbide (SiC). The SiC technology is quite mature, especially for the Schottky diodes, and can withstand voltages from approximately $600\,\mathrm{V}$ to few kilo Volts. The GaN one is less mature, uses HEMT transistors instead of MOS ones, and withstands less voltages, from approx $100\,\mathrm{V}$ to $600\,\mathrm{V}$. They present less capacitance and therefore are suitable for higher frequencies, as high as $20\,\mathrm{MHz}$ if some soft-switching architectures are considered.

The ideal power switch should be able to block high voltages without any leakage current when in the off state, to have zero resistance in the on state, and to have an instantaneous switch on and switch off, without any charge storage.

II. Why do We need Wide Band Gap Semiconductors?

To understand why a Wider Band Gap is favourable the *Baliga's Figure of Merit* is derived with different devices in the following subsections.

A. 1D Abrupt Junction

Starting from the Poisson's equation it is possible to express the electric field $E(x)$, or equivalently the potential $V(x)$, inside the junction (Fig. 1) as follows:

$$E(x) = \frac{-qN_D}{\varepsilon}\left(W_D - x\right), \tag{1a}$$

$$V(x) = \frac{qN_D}{\varepsilon}\left(W_D x - \frac{x^2}{2}\right). \tag{1b}$$

If the device is subject to the breakdown voltage V_{bd}, Eq. (1b) is rewritten as:

$$V_{bd} = \frac{qN_D W_D^2}{2\varepsilon}, \tag{2}$$

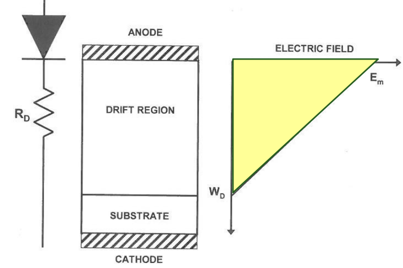


Fig. 1. 1D Abrupt Junction.

and hence

$$W_D = \sqrt{\frac{2\varepsilon V_{bd}}{qN_D}}. \tag{3}$$

The electric field at the interface $E(0)$ if the device is subject to the breakdown (critical field E_C) is then expressed as

$$E(0) = -E_C = \frac{-qN_D W_D}{\varepsilon}, \tag{4}$$

which used in Eq. (2) provides

$$V_{bd} = \frac{E_C W_D}{2}. \tag{5}$$

Now the carrier density can be expressed using Eqs. (3) and (5) as

$$N_D = \frac{\varepsilon E_C^2}{2qV_{bd}}. \tag{6}$$

If the channel resistance is then expressed in terms of its resistivity as

$$R_{on} = \frac{W_D}{qN_D\mu_N}, \tag{7}$$

then

$$R_{on} = \frac{W_D^2}{\mu_n \varepsilon E_C} = \frac{4V_{bd}^2}{\mu_n \varepsilon E_C^3}. \tag{8}$$

The Baliga FoM is a metric to compare different materials for uni-polar power device technology. It considers the drift electron mobility, without taking into account the doping, and the critical electric field.

B. 2D Resurf Junction

The use of a different diode structure allows the design of novel high voltage devices even with very thin epitaxial or implanted layers. The new structure has crucial changes in the electric field distribution near the surface and hence the acronym RESURF (REduced SURface Field) [1].

The basic structure consists of a high-ohmic $\mathrm{P^-}$substrate with an epitaxial $\mathrm{N^-}$layer on it, which is laterally bounded by

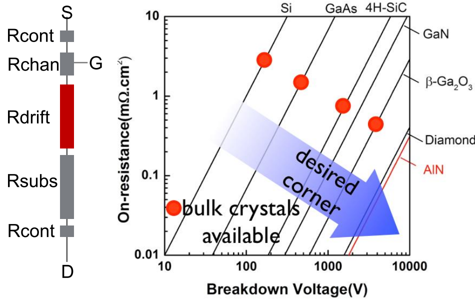


Fig. 2. 1D Abrupt Junction Baliga FoM.

a P^+diffusion. The diode thus formed consists of two parts: one horizontal P^-N junction and a vertical P^+N junction.

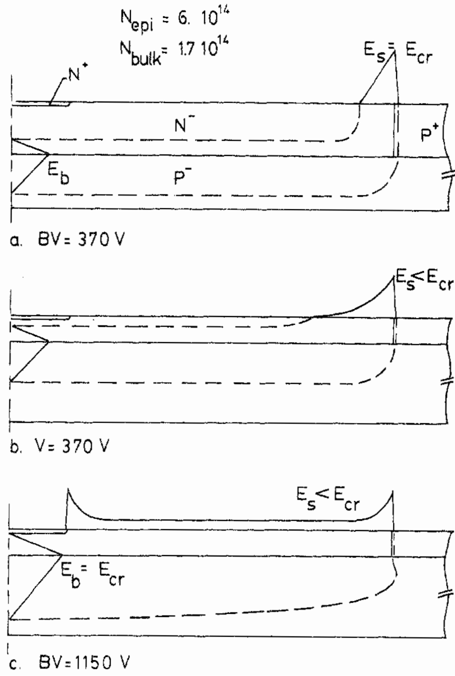


Fig. 3. Representation of the electric field distribution [1].
a. for a thick epitaxial layer (370 V). b. for a thin epitaxial layer (370 V). c. for a thin epitaxial layer (1150 V).

For thick epitaxial layers the depletion at the surface of the vertical P^+N junction is not influenced by the horizontal junction and hence breakdown voltage is determined by the P^+N junction. The electric field pattern along the surface and the axis of symmetry for this case is given in Fig. 3a. Going to thinner layers however, the depletion of the vertical P^+N junction becomes more and more reinforced by the horizontal junction. Consequently, at the same applied voltage, the depletion stretches along the surface over a much longer distance than would be expected according to a simple one-dimensional calculation. Now the electric field at the surface is far below the critical field (Fig. 3b) and a much higher voltage can be applied before breakdown occurs. Beneath a certain thickness of the epitaxial layer, this REduced SURface Field will not reach the critical value not even at high voltages and hence surface breakdown has been eliminated.

Now the breakdown of the diode is determined by the horizontal junction and thus the ideal bulk breakdown can be reached (Fig. 3c). However, since the epitaxial layer is fully depleted, a new effect arises. Due to the curvature of the N^+ contact the electric field will strongly increase. For very thin epitaxial layers the effect becomes so pronounced that the electric field peak at the edge of the N^+ region is larger than the field in the bulk. Now corner breakdown will occur at a voltage which is lower than the ideal bulk breakdown voltage.

The Baliga's FoM for the Resurf junction can be also simply derived without considering the corner breakdown. Starting

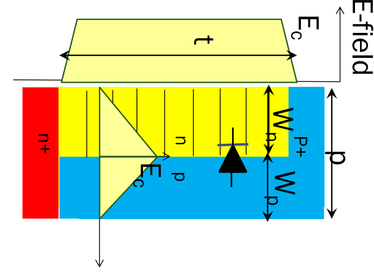


Fig. 4. 2D Resurf Junction.

again from the Poisson's equation it is possible to express the critical electric field $E_C(W_n, W_p)$ of the junction as follows:

$$E_C = \frac{qN_nW_n}{\varepsilon} + \frac{qN_pW_p}{\varepsilon}, \tag{9}$$

hence it is composed by two different field contributions from the vertical and the horizontal junctions. Simplifying with $N_n = N_p$ and $W_n = W_p$,

$$E_C = 2\frac{qN_nW_n}{\varepsilon}. \tag{10}$$

If the channel resistance is then expressed in terms of its resistivity as

$$R_{on} = \frac{1}{qN_n\mu_n}\frac{p}{W_n}t, \tag{11}$$

and the field inside the N region is constant, the breakdown voltage is expressed as $V_{bd} = E_Ct$, and therefore using Eq. (10):

$$R_{on} = \frac{pV_{bd}}{E_CqN_nW_n\mu_n} = \frac{2pV_{bd}}{E_C^2\varepsilon\mu_n}. \tag{12}$$

The Resurf limit depends on the device pitch, hence on the process capabilities.

C. High Electron Mobility Transistor (HEMT)

The High Electron Mobility Transistors is a field-effect transistor incorporating a junction between two materials with different band gaps, a heterojunction, as the channel instead of a doped region. They feature a Low Ron, due to high 2DEG density, High Mobility, high breakdown voltage, because of the GaN high band gap, low capacitance, because there is not any junction to be depleted, and high speed, since it is a majority carrier device.

Polarity of a molecule is a property of the bonds between the atoms making the molecule and refers to the separation of electric charge leading to a presence of an electric dipole.

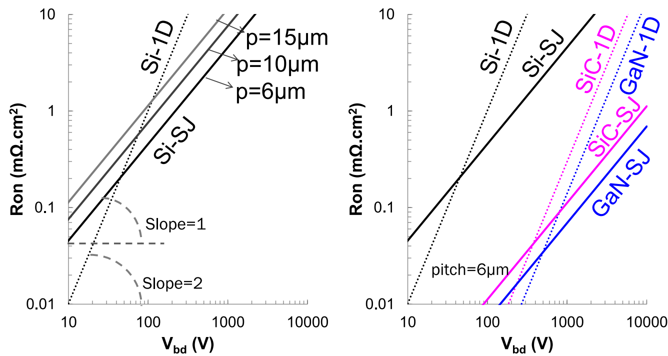


Fig. 5. Baliga FoM for Resurf devices.

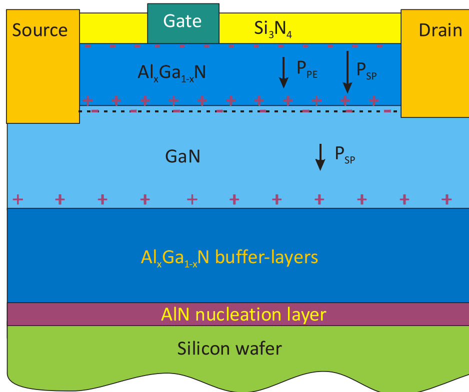


Fig. 6. HEMT stack.

Polarity is attributed to the difference in electro-negativity of atoms in a molecule. In non-polar molecules, the electric charges between the atoms in the molecule are equally distributed due to similar levels of attraction for the charges, as in the centres of their charges coincide. The lack of polarity in non-polar molecules can be a result of a non-polar bond, as in the case of Hydrogen or Silicon, or also due to the symmetry of its structure, as is the case with Carbon Dioxide, which are cancelled due to its symmetrical structure. Meanwhile in contrast to non-polar molecules, in polar molecules the centres of the positive and the negative charges do not coincide and they are separated. A polar molecule has a net dipole as a result of opposing charges due to asymmetrical bonds. Examples of polar molecules are water and GaN. In the absence of an electric field, the electric dipole moment of the molecules is oriented randomly throughout the material and due to this random thermal agitation of molecules, there is no net direction and as a result no net polarity. In the presence of an electric field, the dipole moment attracts and affects the orientation of the polar bond which is aligned in the direction of the electric field.

If a GaN crystal is considered, the Poisson equation yields a surface charge and therefore a polarization field. Then, since the AlGaN has a larger polarization field than GaN due to its higher difference in electro-negativity and to the strain which induces additional charges, when they are connected a large net positive charge would arise in the interface. In GaN HEMTs, the 2DEG is not induced by doping but instead by donor-like surface states on the AlGaN layer facilitated by spontaneous and piezoelectric electric field in the AlGaN layer. The 2DEG density in GaN-based HEMTs is therefore a strong function of the barrier layer (AlGaN) thickness.

The operation of the device requires a gate electrode to control the 2DEG density and hence modulate the drain to source current. Since the 2DEG exists due to the heterostructure, a negative gate voltage is required to deplete it under the gate and hence cut-off current flow. Therefore, GaN HEMTs without special gate stack engineering are normally-on, or depletion devices. Confinement of electrons in the quantum well and absence of dopant in the channel result in high mobility and peak velocity.

The source of the mobile electrons in the 2DEG is still a point of debate. In the absence of a metallic contact on the surface of the device a sheet charge of surface states supply electrons, otherwise the n-doped AlGaN layer, or carrier injection from the gate, supply electrons. The 2DEG serves as a current channel that facilitates a high current density. The electron concentration is mainly determined by conduction band offset, the doping concentration in the barrier layer(s) and the polarization effects.

In the ideal case, without any surface traps, solving the 2D Poisson equation leads to a 2DHG at the SiN/AlGaN interface and no 2DEG at the AlGaN/GaN interface, but it is not corresponding to the reality and needs surface traps to explain the behaviour. The Donor State Model is able to give the right behaviour, but it is still a model and with rather weak direct experimental evidence. By providing some surface donors at the Nitride-AlGaN interface, the 2DHG disappears and the 2DEG comes in, resulting in the desired behaviour.

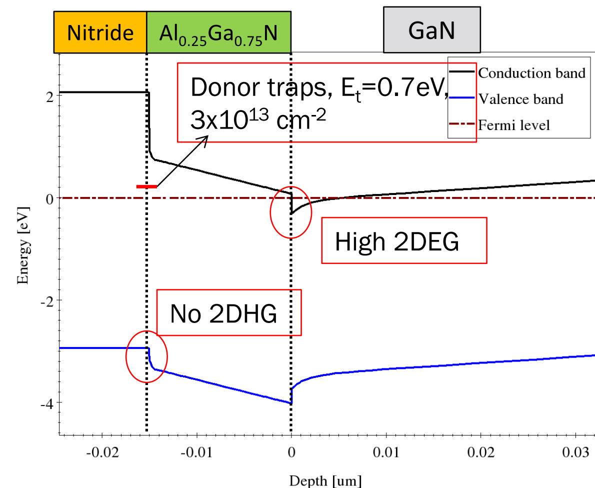


Fig. 7. HEMT band diagram with surface donors.

In order to have a Enhancement GaN HEMT, one possible solution is to employ a pGaN gate, which removes the 2DEG at equilibrium.

The R_{on} can be obtained considering that the semiconductor is undoped and thus behaves as a dielectric, with a rectangular electric field. Therefore, $R_{on} = R_s A$, where R_s is the

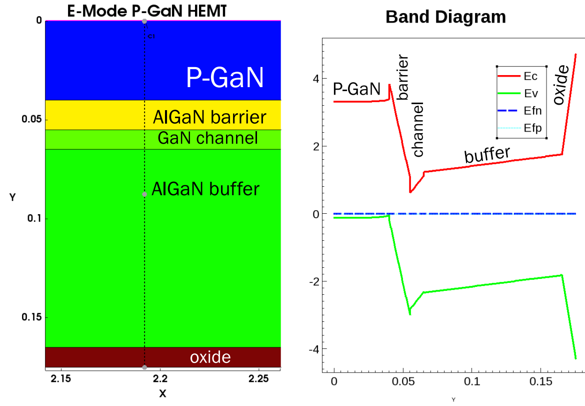
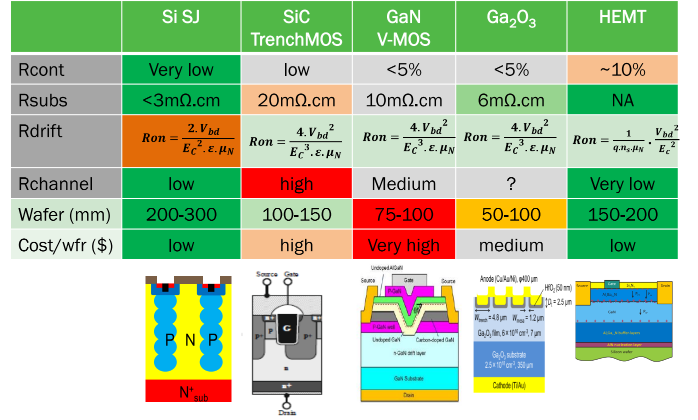


Fig. 8. pGaN stack with band diagram. The pGaN HEMT is an enhancement device.



	Si SJ	SiC TrenchMOS	GaN V-MOS	Ga_2O_3	HEMT
Rcont	Very low	low	<5%	<5%	~10%
Rsubs	<3mΩ.cm	20mΩ.cm	10mΩ.cm	6mΩ.cm	NA
Rdrift	$Ron=\frac{2.V_{bd}}{E_C^2.\varepsilon.\mu_N}$	$Ron=\frac{4.V_{bd}^2}{E_C^3.\varepsilon.\mu_N}$	$Ron=\frac{4.V_{bd}^2}{E_C^3.\varepsilon.\mu_N}$	$Ron=\frac{4.V_{bd}^2}{E_C^3.\varepsilon.\mu_N}$	$Ron=\frac{1}{q.n_s.\mu_N}.\frac{V_{bd}^2}{E_c^2}$
Rchannel	low	high	Medium	?	Very low
Wafer (mm)	200-300	100-150	75-100	50-100	150-200
Cost/wfr ($)	low	high	Very high	medium	low

Fig. 10. Baliga FoM with additional parameters.

resistance of a fixed square and A its area. Then

$$R_{on} = \frac{1}{qn_s\mu_N}\frac{V_{bd}^2}{E_C^2}, \tag{13}$$

or considered that some surface field shaping and dynamic effects might result in more triangular electric field,

$$R_{on} = \frac{4}{qn_s\mu_N}\frac{V_{bd}^2}{E_C^2}. \tag{14}$$

AlGaN/GaN HEMT with rectangular field is hence able to go beyond the 1D GaN limit.

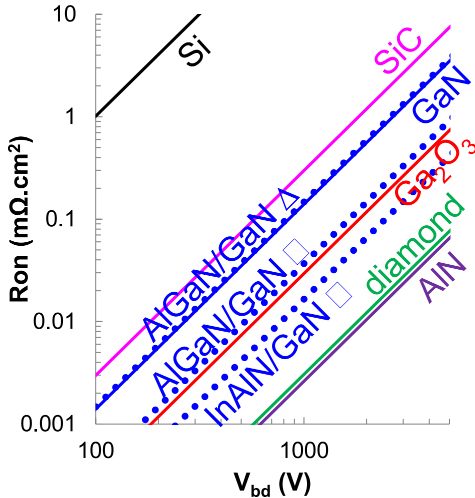


Fig. 9. Baliga FoM for HEMT devices.

D. The Baliga FoM Revisited

The Baliga FoM only refer to the drift region, but the transistor has also the contacts to the pins, a channel to switch the transistor on and off and a substrate. It may be also modified by adding the costs, which is referenced in Fig. 10.

III. Class E ZVS Inverter

The Class E Zero Voltage Switching (ZVS) inverter [2]–[5] belongs to the family of soft-switching inverters, and are the most efficient inverter known so far. The current and voltage waveform of the switch are carefully designed to enable the high efficiency operation by turning on the switch at zero voltage. Since the switch current and voltage waveforms do not overlap during the switching time intervals, switching losses are virtually zero, yielding high efficiency.

In this section, a simple qualitative description of its operation is discussed to provide, albeit simple, insights into the characteristics of this inverter as a basic power cell.

IV. Principle of Operation

The ideal schematic of a Class E inverter is given in Fig. 11. It consists of a power device (an HEMT, or MOSFET, or

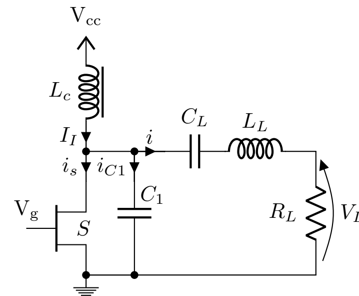


Fig. 11. Class E ZVS inverter.

other suitable ones) operating as a switch, a $L_LC_LR_L$ series-resonant circuit, a shunt capacitor C_1, and a choke inductor L_C. The switch turns on and off at the operating frequency $f = \omega/(2\pi)$ determined by a driver, which has an easy job because it is referenced only to the ground node. Indeed, the bootstrap diode or the floating dc source is not needed, compared to the Class D. The transistor output capacitance, the choke parasitic capacitance, and stray capacitances are included in the shunt capacitance C_1. For high operating frequencies, all of capacitance C_1 can be supplied by the overall shunt parasitic capacitance. The resistor R_L, is an AC load. The

choke inductance L_C is assumed to be high enough so that the AC ripple on the DC supply current can be neglected.

When the switch is ON, the resonant circuit consists of L_L, C_L and R_L, because the capacitance C_1 is short-circuited by the switch. However, when the switch is OFF, the resonant circuit consists of L_L, C_1, C_L and R_L connected in series. Because C_1 and C_L are connected in series, the equivalent capacitance $C_{eq} = C_L C_1/(C_L + C_1)$ is lower than C_L and C_1. The load network is therefore characterized by two resonant frequencies and two loaded quality factors. When the switch is ON,

$$f_{o1} = \frac{1}{2\pi\sqrt{L_L C_L}},\ Q_{L1} = \frac{\omega_{o1} L_L}{R_L} = \frac{1}{\omega_{o1} C_L R_L}. \quad (15)$$

When the switch is OFF,

$$f_{o2} = \frac{1}{2\pi\sqrt{\frac{L_L C_L C_1}{C_L + C_1}}},\ Q_{L2} = \frac{\omega_{o2} L_L}{R_L} = \frac{1}{\frac{\omega_{o2} L_L C_L C_1}{C_L + C_1}}. \quad (16)$$

Fig. 12 shows current and voltage waveforms in the Class E ZVS inverter for three cases: $dv_s(\omega t)/d(\omega t) = 0$, $dv_s(\omega t)/d(\omega t) < 0$, $dv_s(\omega t)/d(\omega t) > 0$ at $\omega t = 2\pi$ when the switch turns on. In all three cases, the voltage vs across the switch and the shunt capacitance C_1 is zero when the switch turns on. Therefore, the energy stored in the shunt capacitance C_1 is zero when the switch turns on, yielding zero turn-on switching loss. Thus, the ZVS condition is expressed by:

$$v_s(2\pi) = 0 \quad (17)$$

The choke inductor L_C forces a dc current I_I. To achieve zero-voltage switching turn-on of the switch, the operating frequency $f = \omega/(2\pi)$ should be greater than the resonant frequency $f_{o1} = 1/(2\pi\sqrt{L_L C_L})$, hence $f > f_{o1}$. However, the operating frequency f is usually lower than $f_{o2} = 1/(2\pi\sqrt{L_L C_{eq}})$, hence $f < f_{o2}$. The shape of the waveform of the current i depends on the loaded quality factor Q_L, and if it is high i is approximately sinusoidal. The combination of the choke inductor and the load series-resonant circuit acts as a current source whose current is $I_I - i$. When the switch is ON, the current $I_I - i$ flows through the switch. When the switch is OFF, the current $I_I - i$ flows through capacitor C_1, producing the voltage across shunt capacitor C_1 and the switch and hence shaping its voltage.

Fig. 12(a) shows current and voltage waveforms for optimum operation. In this case, both the switch voltage v_s and its derivative dv_s/dt are zero when the switch turns on. The second condition is given by:

$$\left.\frac{dv_s(\omega t)}{d(\omega t)}\right|_{\omega t = 2\pi} = 0 \quad (18)$$

The first condition is called zero-voltage switching (ZVS), and the second one is called zero-derivative switching (ZDS) or zero-slope switching. The two conditions are the “nominal conditions”. The optimum conditions are the operating conditions at which the maximum drain efficiency is achieved. For real components, the optimum conditions are off-nominal conditions. The smaller the parasitic components, the closer are the nominal and optimum operating conditions. Because the derivative of v_s is zero at the time the switch turns on, the

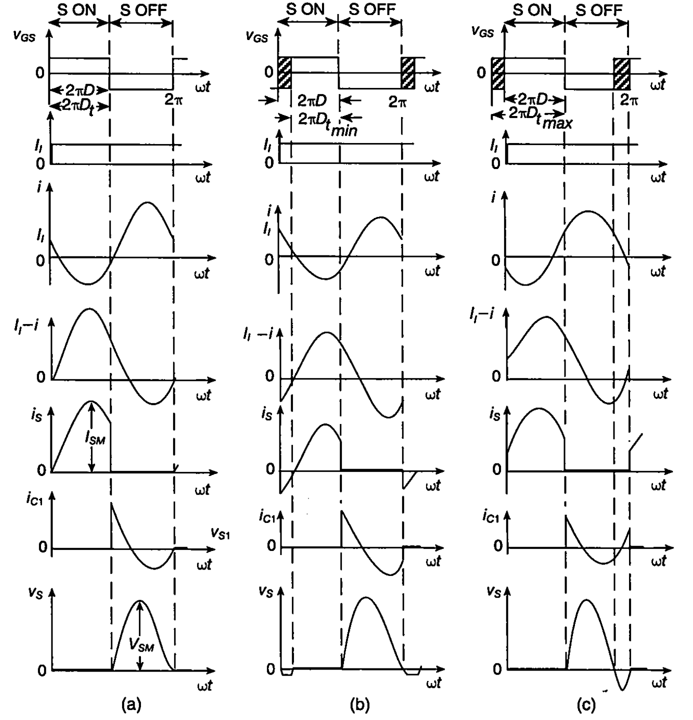


Fig. 12. Waveforms in Class E zero-voltage-switching inverter [3]. (a) For optimum operation. (b) For suboptimum operation with $dv_s(\omega t)/d(\omega t) < 0$ at $\omega t = 2\pi$. (c) For suboptimum operation with $dv_s(\omega t)/d(\omega t) > 0$ at $\omega t = 2\pi$.

switch current is increases gradually from zero after the switch is closed. It should be noted that both the switch voltage and the switch current are positive for optimum operation. Therefore, there is no need to add any diode to the switch. Close relationships among C_1, L_L, R_L, f and the duty-cycle D must be satisfied to achieve optimum operation [6]. Therefore, optimum operation can be achieved only at an optimum load resistance $R_L = R_{L_{opt}}$. If $R_L > R_{L_{opt}}$, the amplitude of the current i through the load series-resonant circuit is lower than that for optimum operation, the voltage drop across the shunt capacitor C_1 decreases, and the switch voltage v_s is greater than zero at turn-on. On the other hand, if $R_L < R_{L_{opt}}$, the amplitude of i is higher than that for optimum operation, the voltage drop across the shunt capacitor C_1 increases, and the switch voltage v_s is less than zero at turn-on. In both cases, the energy in the capacitor C_1 is dissipated in the transistor as heat after the switch is turned on, resulting in a turn-on switching loss. To obtain ZVS operation at a wider load range, an antiparallel or a series diode can be added to the transistor. This improvement ensures that the switch automatically turns on at zero voltage for $R_L < R_{L_{opt}}$.

For operation with zero-derivative switching (ZDS), Miller’s effect is reduced to zero, since instantaneous voltage gain is zero, and therefore the gate-to-drain capacitance reflected to the gate-to-source terminals is C_{gd} and the FET input capacitance is $C_i = C_{iss} = C_{gs} + C_{gd}$. Since Miller’s effect is eliminated and the FET input capacitance is low, the gate-to-source voltage V_G increases much faster than in the inverters with hard switching, in which the slope of the transistor voltage is large when the

transistor turns on.

V. Conclusions

I provided in this report an overview for designing high efficiency power converters and inverters using novel Wide Bandgap Semiconductors, discussing also the advantages by using those power switches. In the second part of report I discussed the basic principles of operating of the class E inverter, which is a layout able to take all the advantages from the properties of the GaN HEMT switches. Indeed, various works in the literature shows high efficiencies, over 90% at the MHz range and hundred of watts, by using the Class E. That inverter with a GaN switch, in a new configuration called Class EF [7] which is able to act as a current source, along with a Class E rectifier with a SiC diode, powered a Position and Load independent Wireless Power Transfer System at 6.78 MHz with a measured constant output voltage of 70 V, a DC-DC peak efficiency of 80% and 100 W in the output. A preliminary conference paper with the design and simulation is in press [8] and an extended version with all the measured data is under-review.

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